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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/876,554	IIDA, IZUO	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-18* is/are pending in the application.

4a) Of the above claim(s) *4-10,17 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 11-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1 and 3-16, drawn to a method of manufacturing a semiconductor device, classified in class 438, subclass 258.

II. Claims 17 and 18, drawn to a device, classified in class 257, subclass 1+.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process. For example, the product as claimed can be made by a process where the oxide film on the floating gate and the gate insulator can be made by separate thermal oxidation steps.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. Newly submitted claims 17 and 18 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: claims 17 and 18 are directed towards a distinct invention of a product.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 17 and 18 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Objections

5. Claims 13-16 are objected to because of the following informalities: Claim 13 line 15 recites "the remaining oxidation-resistant" where it should read "the remaining oxidation-resistant **film**." Claims 14-16 also include this limitation as they depend from claim 13 and are thus also objected to. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 16 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 16 recites the limitation "selectively etching the tunnel insulating film on the region of the semiconductor substrate where the MOS

transistor is to be formed." This limitation was not described in the specification as originally filed. As can be seen in figure 6, the tunnel insulator 16 is not etched in the region of the MOS transistor but instead the gate layer is formed directly on the tunnel insulator layer.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3 and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komori et al. (U.S. Patent No. 5,656,522) in view of Hsieh et al. (U.S. Patent No. 6,165,845).

Komori et al. teaches in figure 4 and on column 5 lines 34-36 and column 8 lines 23-33, a method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate, the method comprising simultaneously forming the oxide film 8 on the floating gate 7a of the non-volatile memory cell transistor and a gate insulating film 8 of the MOS transistor in a single thermal oxidation step. Komori et al. does not teach selectively forming the oxide film on the floating gate.

Hsieh et al. teach a method of fabricating a poly tip in a split-gate flash EEPROM memory cell. Hsieh et al. teach selectively forming the oxide on the floating gate in figure 3f.

Komori et al. and Hsieh et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to selectively form the oxide film on the floating gate. The motivation for doing so is to provide a gate bird's beak to enhance Fowler-Nordheim tunneling for the programming and erasing of the cell. Therefore, it would have been obvious to combine Komori et al. with Hsieh et al. to obtain the invention of claim 1.

With regard to claim 11, Komori et al. teach a method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate. Specifically, Komori et al. teach forming a silicon layer 7a on the substrate 1 (figure 3, column 8 lines 9-21), selectively removing the silicon layer on a region of the substrate where the MOS transistor is to be formed (figure 3, column 8 lines 9-21), and simultaneously forming an oxide film 8 on the region where the floating gate is to be formed and a gate insulating film 8 on the region where the MOS transistor is to be formed (figure 4). Komori et al. do not teach forming an oxidation-resistant film over a first entire resulting surface, selectively removing the oxidation resistant film on the region of the substrate where the MOS transistor is to be formed and on a region of the substrate where the floating gate of the non-volatile memory cell transistor is to be

formed, selectively forming the oxide film on the region where the floating gate is to be formed, or forming a tunneling insulating film over the gate insulating film.

Hsieh et al. teach a method of fabricating a poly tip in a split-gate flash EEPROM memory cell. Hsieh et al. teach forming an oxidation resistant film 50 over a first entire surface (figure 2b) and selectively removing the oxidation-resistant layer on the region where the floating gate of the non-volatile memory cell transistor is to be formed (figure 2c). Hsieh et al. then teach selectively forming an oxide film 45 on the region where the floating gate is to be formed (figure 2d) and forming a tunneling insulating film 50 over the gate insulating film 45 (figure 2f). In combining the two references, it would be obvious to one of ordinary skill in the art a the time of the invention that the oxidation resistant film would be selectively removed on the region where the gate insulating film of the MOS transistor is to be formed as the process of Komori et al. teach forming the oxide on the floating gate and the gate insulating film of the MOS transistor in the same oxidation step.

Komori et al. and Hsieh et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an oxidation resistant film on the entire surface and selectively remove the oxidation-resistant film where the floating gate is to be formed and where the MOS transistor is to be formed, to selectively form the oxide where the floating gate is to be formed, and to form a tunneling insulator over the gate insulating film. The motivation for doing so is to provide a gate bird's beak on the floating gate to enhance Fowler-Nordheim tunneling for the programming and erasing of the cell and to

form the tunneling insulator to insulate the control gate from the floating gate. Therefore, it would have been obvious to combine Komori et al. with Hsieh et al. to obtain the invention of claim 11.

With regard to claim 3, the oxidation resistant film of Hsieh et al. is taught as a silicon nitride film.

With regard to claim 12, the oxide film is formed by a single thermal oxidation step as taught by Komori et al.

With regard to claim 13, Komori et al. teach a method of manufacturing a semiconductor device having a non-volatile memory cell transistor with a control gate stacked on a floating gate through an oxide film and a MOS transistor on the same semiconductor substrate. Specifically, Komori et al. teach forming a first gate insulating film 6 on the semiconductor substrate 1 (figure 2), forming a silicon layer 7a on the first gate insulating film 6 (figure 3, column 8 lines 9-21), selectively removing the silicon layer on a region of the substrate where the MOS transistor is to be formed (figure 3, column 8 lines 9-21), and simultaneously forming an oxide film 8 on the region where the floating gate is to be formed and a second gate insulating film 8 on the region where the MOS transistor is to be formed (figure 4). Komori et al. do not teach forming an oxidation-resistant film over a first entire resulting surface, selectively removing the oxidation resistant film on the region of the substrate where the MOS transistor is to be formed and on a region of the substrate where the floating gate of the non-volatile memory cell transistor is to be formed, selectively forming the oxide film on the region

where the floating gate is to be formed, removing at least some of the remaining oxidation-resistant film, or forming a tunneling insulating film over the gate insulating film.

Hsieh et al. teach a method of fabricating a poly tip in a split-gate flash EEPROM memory cell. Hsieh et al. teach forming an oxidation resistant film 50 over a first entire surface (figure 2b) and selectively removing the oxidation-resistant layer on the region where the floating gate of the non-volatile memory cell transistor is to be formed (figure 2c). Hsieh et al. then teach selectively forming an oxide film 45 on the region where the floating gate is to be formed (figure 2d), removing at least some of the remaining oxidation-resistant film (figure 2e) and forming a tunneling insulating film 50 over the gate insulating film 45 (figure 2f). In combining the two references, it would be obvious to one of ordinary skill in the art a the time of the invention that the oxidation resistant film would be selectively removed on the region where the gate insulating film of the MOS transistor is to be formed as the process of Komori et al. teach forming the oxide on the floating gate and the gate insulating film of the MOS transistor in the same oxidation step.

Komori et al. and Hsieh et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an oxidation resistant film on the entire surface, selectively remove the oxidation-resistant film where the floating gate is to be formed and where the MOS transistor is to be formed, selectively form the oxide where the floating gate is to be formed, remove at least some of the remaining oxidation-resistant

film, and form a tunneling insulator over the gate insulating film. The motivation for doing so is to provide a gate bird's beak on the floating gate to enhance Fowler-Nordheim tunneling for the programming and erasing of the cell and to form the tunneling insulator to insulate the control gate from the floating gate. Therefore, it would have been obvious to combine Komori et al. with Hsieh et al. to obtain the invention of claim 13.

With regard to claim 14, the oxidation-resistant film of Hsieh et al. is taught as a silicon nitride film.

With regard to claim 15, the oxide film is formed by a single thermal oxidation step as taught by Komori et al.

Response to Arguments

10. Applicant's arguments filed 5/5/03 have been fully considered. Applicant's arguments with regard to the 35 U.S.C. 102 rejection of claim 1 are moot in view of the new grounds of rejection presented. Applicant's arguments with regards to the previous 35 U.S.C. 103 (a) rejections have been fully considered but they are not persuasive. Applicant has argued that neither Komori et al. nor Hsieh et al. alone or in combination teach simultaneously and selectively forming the oxide film on the floating gate and a gate insulating film for the MOS transistor. This is not persuasive as Komori et al. combined with Hseih et al. do teach the simultaneous and selective oxidation. Komori et al. teaches simultaneously forming an oxide on the floating gate and a gate insulating film for the MOS transistor in a single step. Hsieh et al. teaches forming the oxide on

the floating gate by a selective oxidation process. The selective oxidation of Hsieh et al. is properly combinable with Komori et al. to teach the claimed invention.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (703) 306-5946. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NDR
June 28, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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